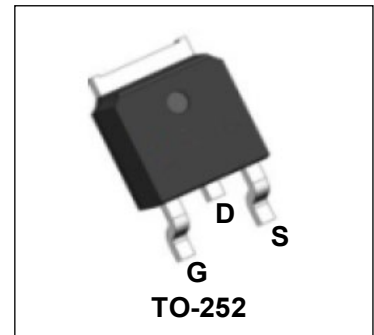


100V N-Channel Enhancement Mode Power MOSFET

Description

WMO099N10LGS uses Wayon's 2nd generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

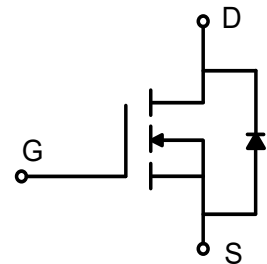


Features

- $V_{DS} = 100V$, $I_D = 67A$
 $R_{DS(on)} < 9.9m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} < 14m\Omega @ V_{GS} = 4.5V$
- Green Device Available
- Low Gate Charge
- 100% EAS Guaranteed

Applications

- DC/DC Converter
- Synchronous Rectification



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ C$	I_D	67	A
	$T_C = 100^\circ C$		43	
Pulsed Drain Current ²		I_{DM}	268	A
Single Pulse Avalanche Energy ³		EAS	180	mJ
Total Power Dissipation ⁴	$T_C = 25^\circ C$	P_D	89.3	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	$R_{\theta JA}$	57	$^\circ C/W$
Thermal Resistance from Junction-to-Case ¹	$R_{\theta JC}$	1.4	$^\circ C/W$

Electrical Characteristics $T_c = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static Characteristics							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V	
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	$T_J = 25^\circ\text{C}$	-	-	1	μA
			$T_J = 100^\circ\text{C}$	-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	-	2.5	V	
Drain-Source on-Resistance ²	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	7.8	9.9	m Ω	
		$V_{GS} = 4.5V, I_D = 10A$	-	11	14		
Forward Transconductance ²	g_{fs}	$V_{DS} = 10V, I_D = 20A$	-	58	-	S	
Dynamic Characteristics							
Input Capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V, f = 1\text{MHz}$	-	3345	-	pF	
Output Capacitance	C_{oss}		-	285	-		
Reverse Transfer Capacitance	C_{rss}		-	19	-		
Switching Characteristics							
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$	-	1.3	-	Ω	
Total Gate Charge	Q_g	$V_{GS} = 10V, V_{DS} = 50V, I_D = 20A$	-	59	-	nC	
Gate-Source Charge	Q_{gs}		-	9.5	-		
Gate-Drain Charge	Q_{gd}		-	13.8	-		
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DS} = 50V, R_G = 3\Omega, I_D = 20A$	-	14.2	-	ns	
Rise Time	t_r		-	28.5	-		
Turn-off Delay Time	$t_{d(off)}$		-	57.6	-		
Fall Time	t_f		-	13.3	-		
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ²	V_{SD}	$I_F = 20A, V_{GS} = 0V$	-	-	1.2	V	
Continuous Source Current ^{1,5}	I_S	$V_G = V_D = 0V$, Force Current	-	-	67	A	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20A, di/dt = 200A/\mu s$	-	34	-	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	55	-	nC	

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.4mH, I_{AS} = 30A$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

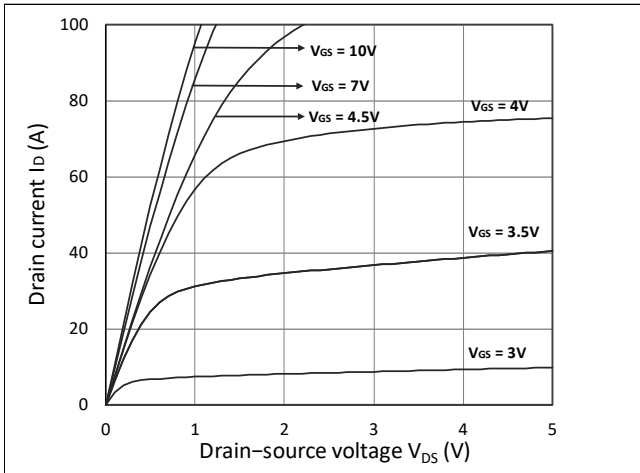


Figure 1. Output Characteristics

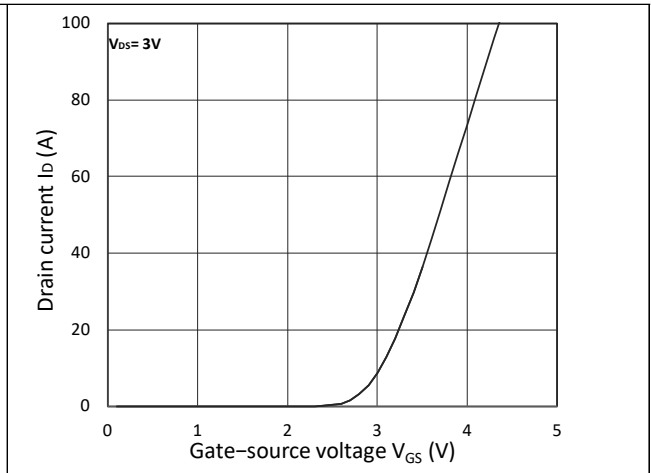


Figure 2. Transfer Characteristics

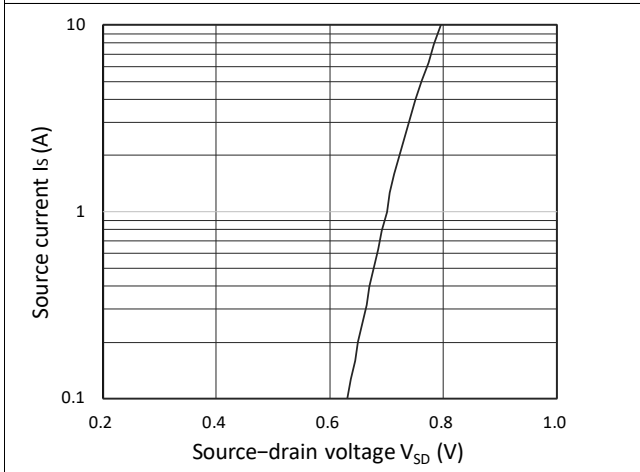


Figure 3. Forward Characteristics of Reverse

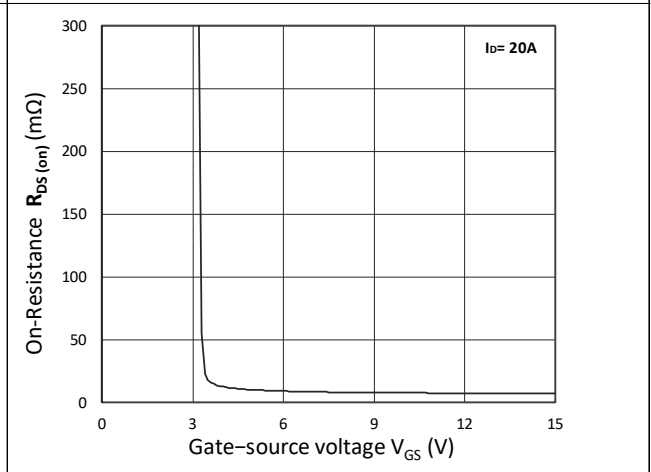


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

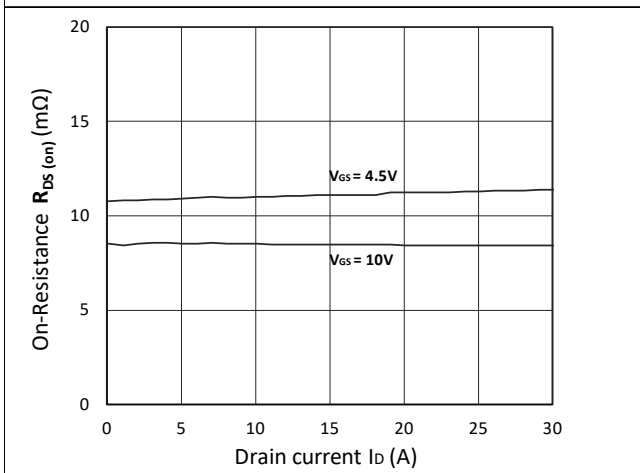


Figure 5. $R_{DS(ON)}$ vs. I_D

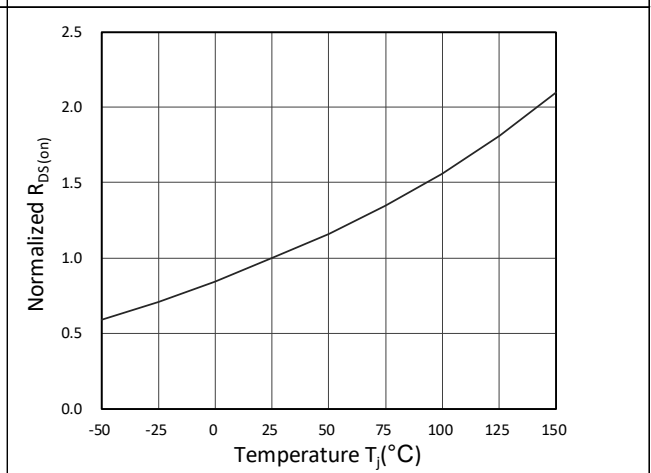


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

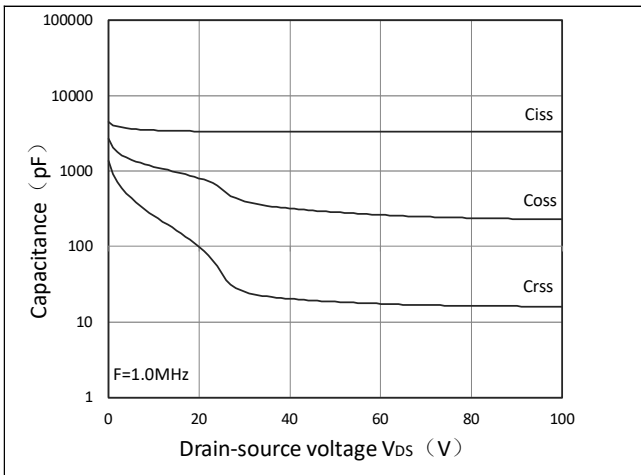


Figure 7. Capacitance Characteristics

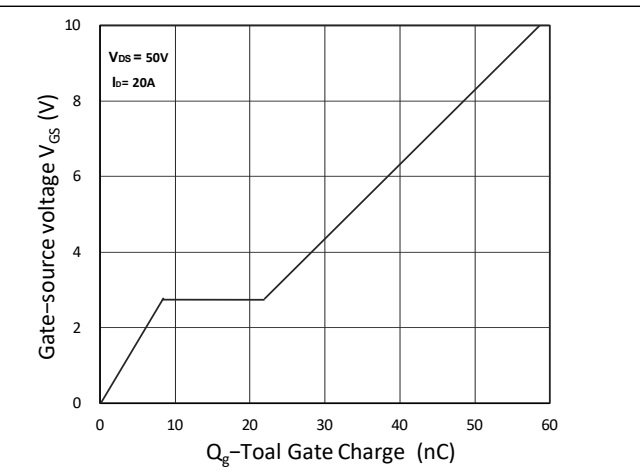


Figure 8. Gate Charge Characteristics

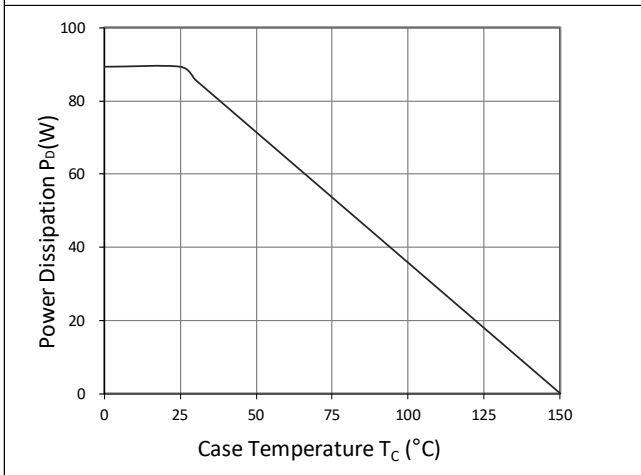


Figure 9. Power Dissipation

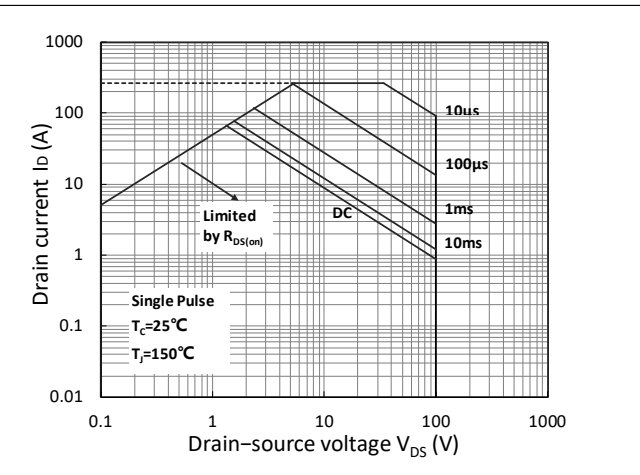


Figure 10. Safe Operating Area

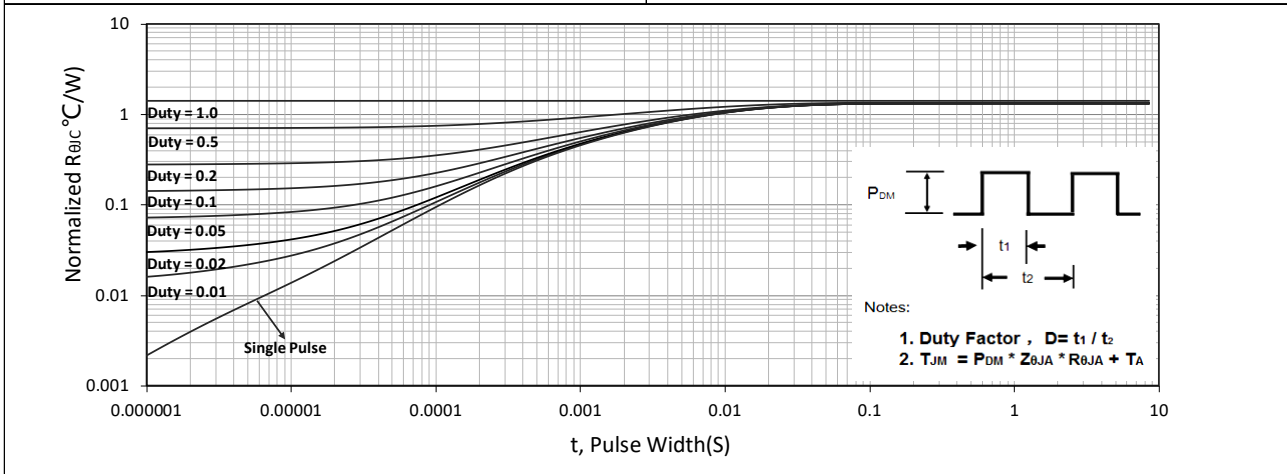


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

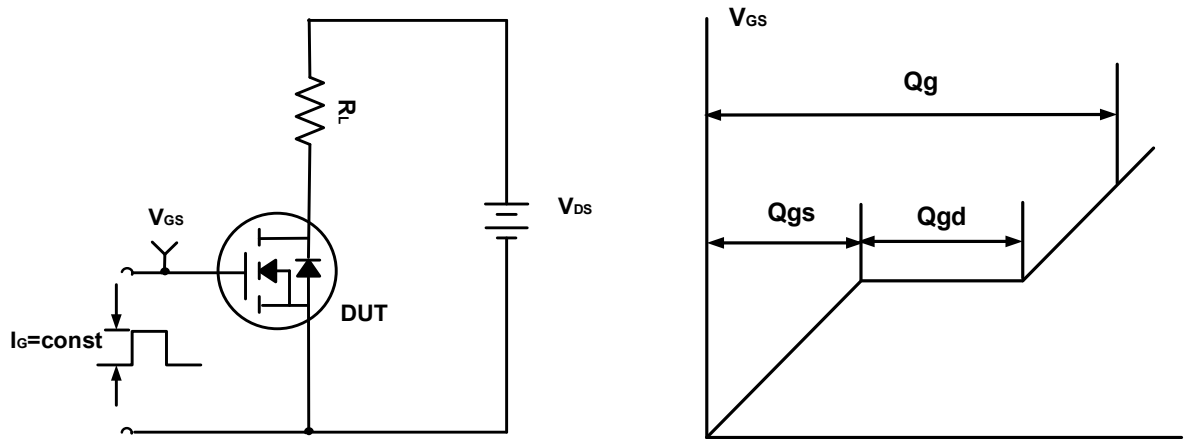


Figure A. Gate Charge Test Circuit & Waveforms

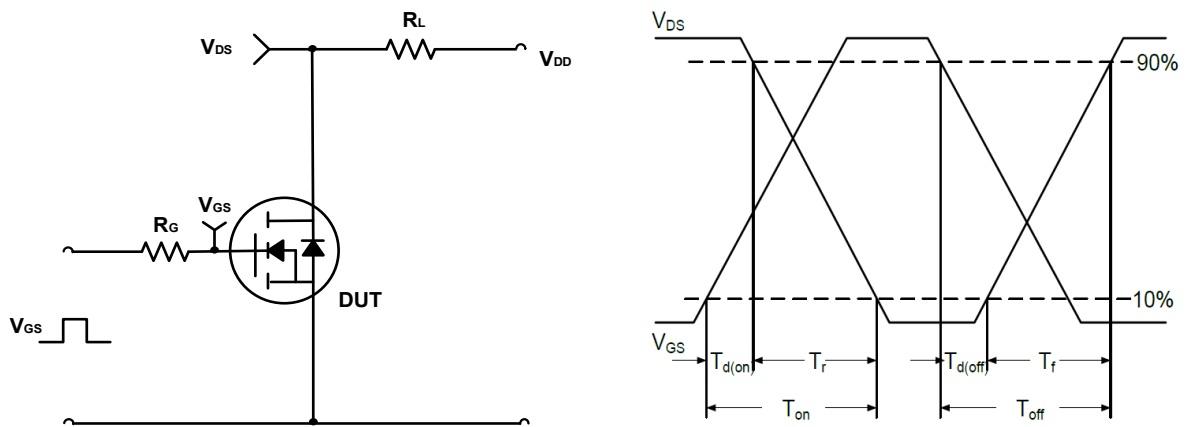


Figure B. Switching Test Circuit & Waveforms

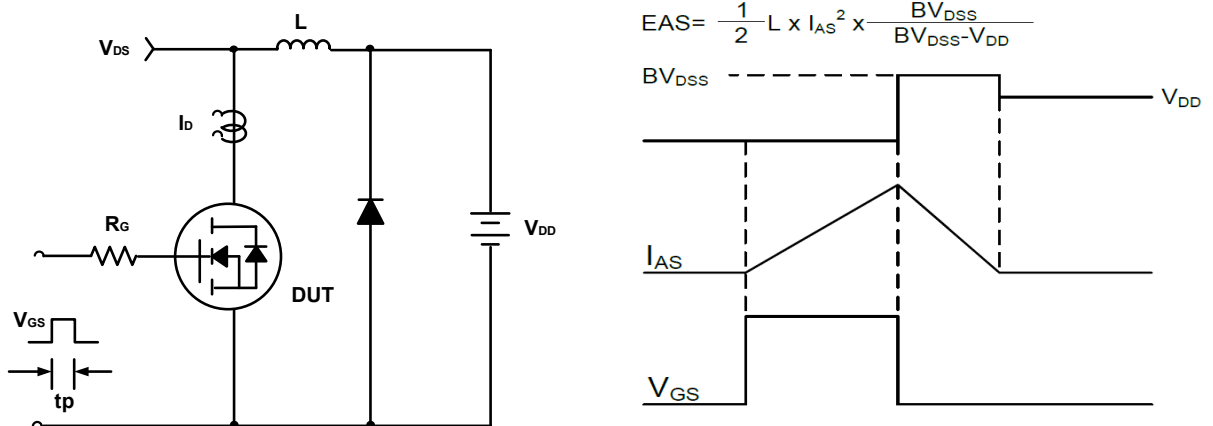
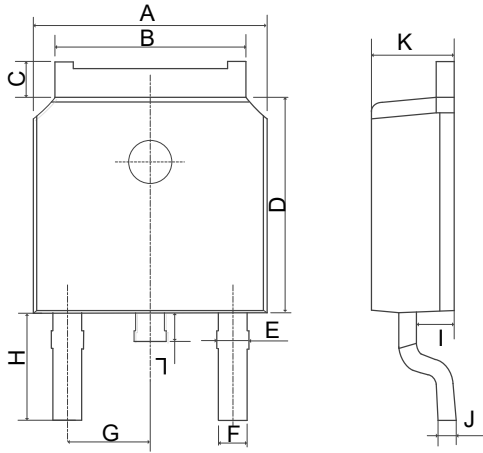


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for TO-252

COMMON DIMENSIONS

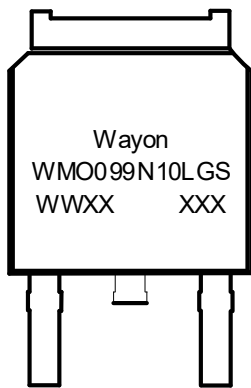


SYMBOL	MM	
	MIN	MAX
A	6.40	6.80
B	5.13	5.50
C	0.88	1.28
D	5.90	6.22
E	0.68	1.10
F	0.68	0.91
G	2.29REF	
H	2.90REF	
I	0.85	1.17
J	0.51REF	
K	2.10	2.50
L	0.40	1.00

Ordering Information

Part	Package	Marking	Packing method
WMO099N10LGS	TO-252	WMO099N10LGS	Tape and Reel

Marking Information



WMO099N10LGS = Device code

WWXX XXX= Date code


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